REMARKS

Claims 1-18 are pending in the application. By this amendment, claims 1, 5, 7, 9, 11, 12, 14, 16 and 17 are being amended to advance the prosecution of the application; marked up versions of amended claims are attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii). No new matter is involved. Reconsideration and allowance are respectfully requested.

In paragraph 2 on page 2 of the Office Action, claims 5, 6, 11, 12, 16 and 17 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. The specific reasons are set forth thereafter. In response thereto, applicant is amending the claims as necessary so as to remove the indefiniteness. In the case of claim 5, for example, such claim recites "wherein silicon nitride layers formed by a CVD method have a given trap density," with the silicon nitride layer subsequently being recited as "having a lower trap density than that of said given trap density." Claims 11 and 12 are being amended to recite a second silicon nitride layer to give meaning to the subsequent reference to "double-layered." Claims 11 and 12 depend from claim 9 which is also being amended to more correctly recite a silicon "nitride" layer. Also, claim 9 is being amended to recite "wherein silicon nitride layers formed by a CVD method have a given trap density" in connection with the subsequent recitation of the silicon nitride layer "having a lower trap density than that of said given trap density." Claim 14 is being amended to more correctly recite a silicon "nitride" layer, and claims 16 and 17 which depend therefrom are being amended by adding the recitation of a second silicon nitride layer so as to give further meaning

to the subsequent recitation "double-layered." Therefore, claims 5, 6, 11, 12, 16 and 17 are submitted to be clear and definite. The typographical error "insulting" is being corrected to --insulating-- in several of the claims.

In paragraph 3 which begins on page 3 of the Office Action, claims 1-4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,661,056 of Takeuchi, Klein et al., Yamada (JP 358106873A) and Wang et al. Takeuchi is said to disclose a non-volatile semiconductor memory device as generally set forth in the claims, with the remaining references being relied upon for their alleged disclosure of features such as the trap density and hydrogen content recited in the various claims. In paragraph 4 which begins at the top of page 6 of the Office Action, claims 7 and 8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi in view of Yamada and further in view of Araki et al. In paragraph 5 which begins on page 8 of the Office Action, claims 9, 10 and 14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi in view of Klein et al. and further in view of Araki et al. In paragraph 6 which begins on page 10 of the Office Action, claims 13, 15 and 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi in view of Klein et al. and further in view of Araki et al., and still further in view of U.S. Patent 5,793,081 of Tomioka. These rejections are respectfully traversed.

The present invention provides a non-volatile semiconductor memory device having an inter-layer insulating layer 15 comprising, for example, a silicon oxide layer 15a, a first silicon nitride layer 15b and a second silicon nitride layer 15c. The

layer 15c is formed by, for example, a JVD method. The inter-layer insulating layer 15 is remarkably different from anything discussed in the cited references. More particularly, the silicon oxide layer 15a contacts the floating gate 14, the first silicon nitride layer is formed by a LPCVD method and exhibits a high trap density, and the second silicon nitride layer 15c exhibits a low trap density and/or low hydrogen density and contacts control gate 16. Because such a structure (the layer 15c, for example, exhibits a low trap density and/or a low hydrogen density) is employed in accordance with the present invention, it is possible to use the inter-layer insulating layer 15 as an inter-layer insulating layer between the floating gate 14 and the control gate 16. Such features in accordance with the invention are neither disclosed nor suggested by any of the cited references. Accordingly, it would not be obvious for one skilled in the art to achieve the present invention based on such references.

In terms of particular features according to the invention, a SiN layer formed by a CVD method has a higher hydrogen density than that formed by a LPCVD method, and has a high layer forming rate, as known from the introduction of Wang. Therefore, such a SiN layer obtained by a CVD method is used as a passivation layer or inter-layer insulating layer of portions other than a gate portion, and is not used as a insulating layer of a gate portion (i.e., between a floating gate and a control gate). This is because a SiN layer obtained by a CVD method is not suitable for a thin layer and for a layer with a low hydrogen density.

As disclosed from the specification of the present application, there are several kinds of ONO layers. One of such layers is an ONO layer comprising a silicon nitride layer formed by the usual LPCVD method, which method is different from the method described in Wang or Klein. The other layer is an ONO layer discussed in Takeuchi. However, such conventional ONO layers are not suitable for an inter-layer insulating layer between a floating gate and a control gate. In other words, it is difficult to form the former ONO layer as a thin, effective layer. The latter ONO layer obtained by a LPCVD method, while including less hydrogen than a layer made by a PECVD method, still includes an appreciable amount of hydrogen. Therefore, if the LPCVD layer contacts the floating gate, various problems such as varying threshold voltage of the transistor occur.

In contrast, the present invention provides the remarkable feature that a silicon nitride layer, such as the layer 15c described, with low hydrogen density and/or low trap density, is used as an inter-layer insulating layer between a floating gate and a control gate, together with layers such as 15b and 15d. Features such as the layer 15c, with low hydrogen density and/or low trap density, are not disclosed by any of the cited references.

In structures according to the present invention, various features are possible. It is possible to make the top oxide layer 15c of the inter-layer insulating layer 15 into a layer which exhibits a low trap density or a low conductivity and which has a thin conversion thickness. Also, it is possible to suppress an increase of

a bird's beak at the post oxidation process without adverse effect by forming a layer which exhibits a low trap density just on the floating gate.

Claims 1-18 are submitted to clearly distinguish patentably over the prior art, taken alone or in the attempted combinations thereof.

Claim 1 defines a non-volatile semiconductor memory device comprised of a semiconductor substrate and a memory cell having a floating gate provided through a tunnel insulating layer on the semiconductor substrate and control gate provided through an inter-layer insulating layer on the floating gate. The inter-layer insulating layer is defined as including a silicon oxide layer contiguous to the floating gate, a first silicon nitride layer on the silicon oxide layer and a second silicon nitride layer on the first silicon nitride layer and having a lower trap density than that of the first silicon nitride layer.

Claims 2-4 depend from and further define claim 1. In claim 3, the quantity of hydrogen content of the first silicon nitride layer is defined as being $10^{21}/cm^3$ or more, while in claim 4 the quantity of hydrogen content of the second silicon nitride layer is defined as $10^{19}/cm^3$ or less.

Claim 5 defines a non-volatile semiconductor memory device in terms of the basic combination similar to claim 1, and in which the inter-layer insulating layer is defined as including a silicon oxide layer contiguous to the floating gate and a silicon nitride layer deposited on the silicon oxide layer. Reference is made to silicon nitride layers formed by a CVD method having a given trap density, and the

silicon nitride layer is defined as having a lower trap density than that of the given trap density.

Claim 6 depends from and contains all of the limitations of claim 5.

Claim 7 sets forth the basic combination of claims 1 and 5, and in addition defines the inter-layer insulating layer as including a silicon oxide layer contiguous to the floating gate and a silicon nitride layer deposited on the silicon oxide layer and having a quantity of hydrogen content on the order of $10^{19}/cm^3$ or less.

Claim 8 depends from and contains all of the limitations of claim 7.

Claim 9 defines the basic combination of claims 1, 5 and 7, and defines the inter-layer insulating layer as including a silicon nitride layer serving as a layer contiguous to at least one of the floating gate and the control gate. There is reference to silicon nitride layers formed by a CVD method and having a given trap density, and the silicon nitride layer is defined as having a lower trap density than that of the given trap density.

Claims 10-12 depend from and further define claim 9. In claim 11, the inter-layer insulating layer is defined in terms of first and second silicon nitride layers which are so double-layered as to be contiguous to both of the floating gate and the control gate, and a silicon oxide layer interposed between the double-layered silicon nitride layers. In claim 12, the inter-layer insulating layer is defined in terms of first and second silicon nitride layers that are so double-layered as to be contiguous to both of the floating gate and the control gate in a stack layer consisting of a

silicon oxide layer and silicon nitride layer between the double-layered silicon nitride layers.

Claim 13 depends from and further defines claim 9 in terms of the silicon nitride layer being provided only on the side contiguous to the floating gate, and a silicon oxide layer and a stack layer consisting of a silicon nitride layer and a silicon oxide layer provided on the silicon nitride layer.

Claim 14 sets forth a basic combination similar to claims 1, 5, 7, 9 and 13, and defines the inter-layer insulating layer as including a silicon nitride layer serving as a layer contiguous to at least one of the floating gate and the control gate and having a quantity of hydrogen content on the order of $10^{19}/cm^3$ or less.

Claims 15-18 depend from and further define claim 14. In claim 16, the inter-layer insulating layer is defined in terms of first and second silicon nitride layers which are so double-layered as to be contiguous to both the floating gate and the control gate, and a silicon oxide layer interposed between the double-layered silicon nitride layers. In claim 17, the inter-layer insulating layer is further defined in terms of first and second silicon nitride layers which are so double-layered as to be contiguous to both the floating gate and the control gate, and a stack layer consisting of a silicon oxide layer and a silicon nitride layer between the double-layered silicon nitride layers. Claim 18 further defines the inter-layer insulating layer of claim 14 in terms of the silicon nitride layer being provided only on the side contiguous to the floating gate, and a silicon oxide layer and a stack layer consisting

of a silicon nitride layer and a silicon oxide layer which are provided on the silicon nitride layer.

Thus, each of claims 1-18 clearly distinguishes patentably over the prior art.

In conclusion, the claims as amended herein are submitted to clearly distinguish patentably over the prior art for the reasons set forth above. Therefore, reconsideration and allowance are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

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Version with markings to show changes made:

Rewrite claim 1 as follows:

1. (Amended) A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer [insulting] insulating layer on said floating gate;

wherein said inter-insulating layer includes:

a silicon oxide layer contiguous to said floating gate;

a first silicon nitride layer provided by a CVD method on said silicon oxide layer; and

a second silicon nitride layer provided on said first silicon nitride layer and having a lower trap density than that of said first silicon nitride layer.

Rewrite claim 5 as follows:

5. (Amended) A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer [insulting] insulating layer on said floating gate,

wherein silicon nitride layers formed by a CVD method have a given trap density and said inter-insulating layer includes:

a silicon oxide layer contiguous to said floating gate; and

a silicon nitride layer deposited on said silicon oxide layer and having a lower trap density than that of said [silicon nitride layer formed by a CVD method] given trap density.

Rewrite claim 7 as follows:

7. (Amended) A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer [insulting] insulating layer on said floating gate,

wherein said inter-insulating layer includes:

a silicon oxide layer contiguous to said floating gate; and

a silicon [oxide] nitride layer deposited on said silicon oxide layer and having a quantity of hydrogen content on the order of $10^{19}/cm^3$ or less.

Rewrite claim 9 as follows:

9. (Amended) A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer [insulting] insulating layer on said floating gate,

wherein silicon nitride layers formed by a CVD method have a given trap density and said inter-insulating layer includes:

a silicon [oxide] nitride layer serving as a layer contiguous to at least one of said floating gate and said control gate, and having a lower trap density than that of [a silicon nitride layer formed by a CVD method] said given trap density.

Rewrite claim 11 as follows:

11. (Amended) A non-volatile semiconductor memory device according to claim 9, further including a second silicon nitride layer, and wherein said first-mentioned silicon nitride [layers] layer and said second silicon nitride layer are so double-layered as to be contiguous to both of said floating gate and said control gate, and

still further including a silicon oxide layer [is] interposed [in] between said double-layered silicon nitride layers.

Rewrite claim 12 as follows:

12. (Amended) A non-volatile semiconductor memory device according to claim 9, further including a second silicon nitride layer, and wherein said first-mentioned silicon nitride [layers] layer and said second silicon nitride layer are so double-layered as to be contiguous to both of said floating gate and said control gate, and

still further including a stacked layer consisting of a silicon oxide layer and a silicon nitride layer formed by a CVD method [is] interposed [in] between said double-layered silicon nitride layers.

Rewrite claim 14 as follow:

14. (Amended) A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer [insulting] insulating layer on said floating gate,

wherein said inter-insulating layer includes:

a silicon [oxide] nitride layer serving as a layer contiguous to at least one of said floating gate and said control gate, and having a quantity of hydrogen content on the order of $10^{19}/cm^3$ or less.

Rewrite claim 16 as follows:

16. (Amended) A non-volatile semiconductor memory device according to claim 14, further including a second silicon nitride layer, and wherein said first-mentioned silicon nitride [layers] layer and said second silicon nitride layer are so double-layered as to be contiguous to both of said floating gate and said control gate, and

still further including a silicon oxide layer [is] interposed [in] between said double-layered silicon nitride layers.

Rewrite claim 17 as follows:

17. (Amended) A non-volatile semiconductor memory device according to claim 14, further including a second silicon nitride layer, and wherein said first-mentioned silicon nitride [layers] layer and said second silicon nitride layer are so double-layered as to be contiguous to both of said floating gate and said control gate, and

still further including a stacked layer consisting of a silicon oxide layer and a silicon nitride layer formed by a CVD method [is] interposed [in] between said double-layered silicon nitride layers.